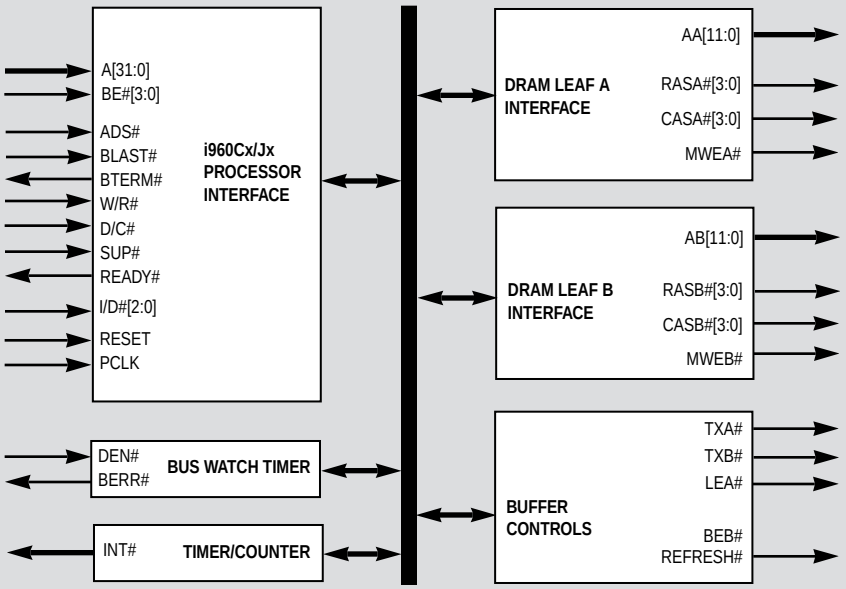
V96BMC High-Performance Memory Controller

- Direct Interface to i960® Cx/Hx Processor
- SRAM Performance Achieved With DRAM
- Supports Up to 512 Mbytes of DRAM
- Non-Interleaved or Two-Way Interleaved Operation
- Square and Rectangular Arrays
- Integrated Page Cache Management
- 1 Kbyte Burst Transaction Support
- Two 24-Bit Timers
- 8-Bit Bus Watch/Timer
- High Speed, Low Power CMOS Technology
- Available in Low-Cost PQFP
- Faster and Less Expensive Than an FPGA Based Design



V96BMC Block Diagram

Typical Application

The V96BMC High-Performance DRAM Controller provides all aspects of DRAM control for high performance systems using i960 Cx/Hx processors. The V96BMC is designed to interface directly to the i960 Cx/Hx processors with no glue logic required. The V96BMC provides the DRAM access protocols, buffer signals, data multiplexer signals and bus timing resources required to work with the latest technology of DRAMs. By using the V96BMC, system designers can replace tedious design work, expensive FPGA's and valuable board space, with a single, high-performance, easily configured device.

The processor interface of the V96BMC implements the bus protocol of the i960 Cx/Hx processor. The pin naming convention has been duplicated on the V96BMC. Simply wire like-named pins together to create the interface.

The V96BMC supports a total DRAM memory subsystem size of 512 Mbytes. The array may be organized as 1 or 2 leaves of 32 bits each. Standard memory sizes of 256 Kbit to 64 Mbit are supported and 8, 16 and 32 accesses are allowed.

The V96BMC takes advantage of fast page mode DRAMs and row comparison logic to achieve static RAM performance using DRAMs.

The V96BMC supplies the control signals needed for external data path buffer components. The use of multi-mode control signals gives the designer flexibility to select buffer components which are optimized for the desired cost and performance. Most standard buffers can be used without external logic.

The V96BMC provides an 8-bit bus watch timer to detect and recover from accesses to unpopulated memory regions. The two 24-bit counter/timers supply an external interrupt signal at a constant frequency relative to the system clock. The V96BMC is packaged in a low-cost 132-pin PQFP package and in a 124-pin PGA package and is available in 16, 25, and 33 MHz versions.

PROCESSORS SUPPORTED:
i960 Cx/Hx Processors

AVAILABILITY:
Now

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